

10/814,943


Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 001207.P011	Application Number: Not yet assigned
	First Named Inventor: Peter M. Pani	
	Filing Date: Herewith	

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Code ²	Kind (If known)			
W		4,912,342		Wong, et al.	3/1990	
		4,918,440		Furtek	4/17/90	
		4,935,734		Austin	6/19/90	
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		5,144,166		Camarota et al.	9/1/92	
		5,187,393		Elgamal et al.	2/16/93	
		5,204,556		Shankar	4/20/93	
		5,208,491		Ebeling, et al.	5/4/93	
W		5,221,865		Phillips, et al.	6/22/93	

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✓		Re 34,363		Freeman	8/1993	
		4,020,469		Manning	4/26/77	
		4,661,901		Veneski	4/28/87	
		4,700,187		Furtek	10/13/87	
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		4,815,003		Putatunda et al.	3/21/89	
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<i>W</i>		5,243,238		Kean	9/7/93	
		5,256,918		Suzuki	10/1993	
		5,260,610		Pederson, et al.	11/9/93	
		5,260,611		Cliff et al.	9/1993	
		5,296,759		Sutherland, et al.	3/22/94	
		5,298,805		Garverick, et al.	3/29/94	
		5,329,470		Sample, et al.	7/12/94	
		5,349,691		Harrison, et al.	9/1994	
		5,369,314		Patel, et al.	11/1994	
<i>W</i>		5,376,844		Pederson et al.	12/1994	

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✓		5,396,126		Britton, et al.	3/7/95	
		5,406,525		Nicholes	4/11/95	
		5,444,394		Watson, et al.	8/1995	
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		5,457,410		Ting	10/10/95	
		5,469,003		Kean	11/21/95	
		5,477,067		Isomura, et al.	12/19/95	
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✓		5,550,782		Cliff, et al.	8/27/96	
		5,552,722		Kean	9/3/96	
		5,572,148		Lytle, et al.	11/5/96	
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		5,894,228		Reddy	4/13/99	
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✓		5,914,616		Young	6/22/99	

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✓		6,016,063		Trimberger	1/2000	
		6,034,547		Pani, et al.	3/7/00	
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		6,693,456		Wong	2/17/04	
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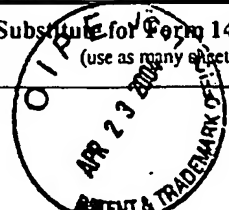
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		Office ³ Code ⁵	Number ⁴	Kind (If known)				
GPO		EPO	0415542		Advanced Micro Devices, Inc.	3/6/91		
		EPO	0630115A2		Pilkington Micro-Electronics Limited	6/1/94		
		PCT	9410754		Xilinx, Inc.	5/11/94		
		PCT	9208286		Concurrent Logic, Inc.	5/14/92		
		PCT	9504404		Advantage Logic, Inc.	2/9/95		
		PCT	9605964		Minnesota Mining and Manufacturing Co.	4/3/96		
		PCT	9635261		BTR, Inc.	11/7/96		
		PCT	9428475		Regents of the University of California	12/8/94		
		PCT	9528769		BTR, Inc.	10/26/95		
		UK	2180382		Pilkington Micro-Electronics Limited	3/25/87		
1/10		UK	2295738		Altera Corporation	5/6/96		

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OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
tan		Altera Corporation Date Sheet, Flex EPF81188 12,000 Gate Programmable Logic Device, September 1992, Ver. 1, pp. 1-20.	
tan		ATMEL Field Programmable Arrays, AT 6000 Series, 1993, p. 1-16. Coproccessor Field Programmable Gate arrays AT 6000 (LV) Series, 10/99, Page 1-27.	
tan		BRITTON, et al., "Optimized Reconfigurable Cell Array Architecture for High-Performance Field Programmable Gate Arrays," Proceedings of the IEEE 1993 Custom Integrated Circuits Conference, 1993, pp. 7.2.1. - 7.2.5. 3/93	
tan		BUFFOLI, E., et al., "Dynamically Reconfigurable Devices Used to Implement a Self-Tuning, High Performances PID Controller," 1989 IEEE, pp., 107-112. 8/89	
tan		BURSKY, D., "Fine-Grain FPGA Architecture Uses Four Levels of Configuration Hierarchy," 2328 Electronic Design, 41, No. 20, Cleveland, OH, October 1, 1993, pp. 33-34.	
tan		Cliff, et al., "A Dual Granularity and Globally Interconnected Architecture for a Programmable Logic Device", IEEE '93 pp. 7.3.1-7.3.5. 3/93	
tan		DEVADES, S., et al., "Boolean Decomposition of Programmable Logic Arrays," IEEE 1988, pp. 2.5.1 - 2.5.5. 1/88	
tan		F. Zlotnick, P. Butler, W. Li, D. Tang, "A High Performance Fine-Grained Approach to SRAM Based FPGAs", p. 321-326, Wescon September 28-30, 1993.	
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tan		Minnick, R.C., "A Survey of Microcellular Research", vol. 14, no. 2, 4/1967, pp. 203-241.	

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UTM		Motorola Project Brief, "MPA10xx Field Programmable Gate Arrays," September 27, 1993, 2 pages.	
UTM		Robert H. Krambeck, "ORCA: A High Performance, Easy to Use SRAM Based Architecture", p. 310-320, Wescon September 28-30, 1993.	
UTM		SHOUP, R. G., "Programmable Cellular Logic Arrays," Abstract, Ph.D. Dissertation, Carnegie Mellon University, Pittsburgh, PA, March 1970, (partial) pp. ii-121.	
UTM		Sinan Kaptanoglu, Greg Bakker, Arun Kundu, Ivan Corneillet, Ben Ting, "A New High Density and Very Low Cost Reprogrammable FPGA Architecture", 10 pages, Actel Corporation. <i>No date.</i>	
UTM		SPANDORFER, L.M., "Synthesis of Logic Functions on an Array of Integrated Circuits," Contract No. AF 19 (628) 2907, Project No. 4645, Task No. 464504, Final Report, November 30, 1965.	
UTM		SUN, Y., et al., "An Area Minimizer for Floorplans with L-Shaped Regions," 1992 International Conference on Computer Design, 1992 IEEE, pp. 383-386. <i>4/92</i>	
UTM		VIDAL, J. J., "Implementing Neural Nets with Programmable Logic," IEEE Transactions on Acoustic, Speech, and Signal Processing, Vol. 36, No. 7, July 1988, pp. 1180-1190.	
UTM		Wang, P. et al. IEEE, "A High Performance FPGA with Hierarchical Interconnection Structure", pp. 239-242 (May 30, 1994).	
		Xilinx, "The Programmable Gate Array Data Book", 1992. <i>only table of contents scanned.</i> <i>UTM</i>	

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<i>JP</i>		6,594,810		Reblewski et al.	7/15/03	<i>✓</i>

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